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30-Bit Oversampling ADC for Low Bandwidth Applications

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ABSTRACT

This research paper presents a 30-bit resolution Fourth order multi bit cascade of multiple feedback (CIFB) delta sigma modulator Analog-to-Digital Converter for Low bandwidth applications. The proposed modulator topology can achieve 29-bit resolution for very small bandwidth application. CIFB topology is considered as a higher stability for the modulator. The signal transfer function response is shown as a low-pass response because delta-sigma modulator is a low pass. The quantization noise shaped in the high pass noise transfer function. The ideal modeling simulation, NTF zeroes which are poles of the loop filter are adjusted at the DC on the unit circle. Due to the fourth-order modulator high out of band gain (OBG) of 4 set to shape more quantization noise from signal band. The NTF zero optimization techniques also employed for higher performance. The proposed modulator design investigated for different higher oversampling ratio like 128, 64, 32. The modulator can achieve fourth-order modulator with 4-bit quantizer can reach signal to noise ratio (SNR) of 123 dB with OSR of 32. The proposed modulator with OSR of 64 can come by SNR of 151 dB. Finally, the modulator can attain SNR of 182 dB for OSR of 131 with full-scale input of the modulator is 550 mV. Due to CIFB topology, higher stability with multiple feedback structure. Now adays there is need of higher gain DC operational amplifier which attains higher resolution. Also, investigate limited DC gain, limited gain bandwidth and slew rate of operational amplifier. Finally, the modulator is simulated for circuit non-idealities of thermal noise and flicker noise.

Keywords: Operational Amplifier, Analog-to-Digital Converter, Digital-to-Analog Converter, Signal-Transfer Function, Noise Transfer Function

1. INTRODUCTION

For having higher speed, higher density and low cost, digital system continuously pushed by scale down of CMOS technology. Generally, technology scaling is related to reduce in supply voltage, which contract the signal swing and circuit dynamic range [1]. By reducing supply voltage, it creates huge difficulties to the design of a high-resolution analog-to-digital converter. Therefore, by increasing demands of the portable battery devices the low power consumption became more censorious in modern integrated circuit design [2]. A fourth-order multi-bit cascade-of-multiple-feedback delta-sigma modulator for Low bandwidth applications. The proposed modulator topology can achieve 30-bit resolution for very small bandwidth application. Recently the delta-sigma modulator gaining popularity for higher signal bandwidth applications. While the continuous-time delta-sigma modulator have key advantages does not require anti-aliasing filter and requires much lower gain-bandwidth. Discreate-time delta-sigma modulator have switched-capacitor implementation with components of capacitor, switches, and operational amplifier as an integrator. The continuous-time implementation uses resistor and capacitor with operational amplifier as integrator. It is well known

that Nyquist pipeline ADC require accurate inter-stage gain, that determine high-gain wideband residue amplifier and calibration technology, leads to complexity and power efficiency employing noise shaping and oversampling. However, the requirement of oversampling ratios, that is typically small [3-6]. The delta-sigma modulator more than 50 MHz getting popularity due to increased demands in portable system. The discrete-time implementation quite popular due to high accuracy but smaller bandwidth. The demand for higher bandwidth rising with increased resolution. The challenges due to smaller OSRs due to the reason of process limited clock rate. To reach sufficient higher dynamic range, higher order noise shaping needs to be implemented by increasing the noise transfer function order, that is conventionally performed by loop filter cascade and generally equal or greater than three or more required. At the same time increased order of the loop filter causes stability issues [7]. A wideband continuous-time third order with 4-bit quantizer delta-sigma modulator designed for signal band of 100MHz can achieve dynamic range of 80-dB in 40 nm CMOS Technology at supply voltage of 1.2 V with power consumption of 69.7 mW. The modulator uses three-stage feedforward amplifier with miller compensation. The first integrator has unity gain bandwidth of 3.6 GHz and phase margin of 57 degree including all loading effect with power consumption of 10.5mW from power supply of 1.2V. The second and third integrator adopts the similar structure of the amplifier with scaled bias currents, that results in achieving unity gain bandwidth of 4.7 GHz and 3.3 GHz respectively. The phase margin for second and third integrator is 58 degree and 57 degrees and consuming power of 4.3mW and 17.3mW respectively. The power breakdown shows that loop filter consumes more than 46% of the powers with total modulator power of 69. 7mW. While the 4-bit quantizer implemented as 4-bit flash ADC with each cell uses preamplifier due to smaller signal swing in front of quantizer. The digital to analog converter is implemented using current steering unit element. Finally, the modulator can achieve signal to noise plus distortion ratio (SNDR) of 76dB and DR of 84 dB for signal bandwidth of 100 MHz for 40 nano-meter CMOS Technology [8]. A modulator with third order loop filter with preliminary sampling and quantization scheme in backend sub-ranging multi-bit quantizer can achieve SNDR of 72 dB for signal bandwidth of 100 MHz. The cascade of integrator with multiple feedforward topology used to take advantage of single DAC. While segmented non-return to zero digital to analog used for feedback. By excessing loop delay compensation implemented around the second integrator. The modulator total power consumption is 16.3mW, while the loop filter integrators consume 9.4mW, DAC consumes 3.5mW, quantizer 1.4mW and CLK and digital consumes 2mW respectively in 28 nm CMOS Technology sampling at 2GS/s. SNDR of 72.6 dB, SNR 73.2 dB and dynamic range of 76.3 dB respectively achieve by modulator for signal bandwidth of 100 MHz in 28nm CMOS Technology [9]. Another high bandwidth CT delta-sigma modulator with signal bandwidth of 125MHz proposed based on VCO based integrators. The modulator uses VCO based quantizer and segmented phase-domain ELD compensation. The loop filter is active RC integrator based, while modulator topology is cascaded of integrator with multiple feedforward. The first integrator operational amplifier unity gain frequency is four times to sampling frequency. The second integrator operational amplifier

sampling frequency is four times to unity gain frequency. Sampling frequency is three times to modulator. Therefore, sampling frequency becomes three times to the unity gain third RC integrator operational amplifier. Finally, the third order modulator with VCO based quantizer can achieve SNDR of 71.9 dB and dynamic range of 74.8dB for signal band of 125MHz with power consumption of 54mW sampling frequency of 2.15GHz with OSR of 8.6 in 16nm CMOS Technology [10]. A CT Multi-stage Noise Shaping modulator designed for signal band of 465MHz in 28 nm CMOS Technology. A 1 to 2 MASH topology is adopted to attain irritating noise shaping with higher stability at much lower OSR of 8.6. The first stage is a first order modulator to reduce the power amplifier for given thermal noise requirement. First stage depends on an active RC integrator, quantizer While second stage consists of an active RC resonator, flash ADC with 17 level capacitive and current steering DAC which is used to provide fast direct feedback. In this work, second stage uses feedback topology to adjust signal transfer function peaking. On the other side the input full-scale of second stage is scaled down to provide an interstage gain of six to reduce the overall QN which prevents the left out of the first stage from saturating second stage [11].

This paper proposed a 30-bit resolution Fourth-order multi-bit cascade-of-multiple-feedback (CIFB) delta-sigma modulator Analog to Digital Converter for Low bandwidth applications. The proposed modulator topology can achieve 29-bit resolution for very small bandwidth application. Consider the higher stability, CIFB topology is considered for the modulator. The low-pass response of the signal transfer function (STF) because the delta-sigma modulator is a low pass. The High pass response shapes quantization noise in the noise transfer function (NTF). Due to ideal modeling simulation, NTF zeroes which are poles of the loop filter are adjusted at the DC on the unit circle. Due to the fourth-order modulator high out of band gain of 4 set to shape more quantization noise from signal band. The NTF zero optimization techniques also performance. The proposed modulator design investigated for different higher oversampling ratio like 128, 64, 32. The modulator can achieve fourth-order modulator with 4-bit quantizer can achieve signal to noise ratio of 123 dB with OSR of 32. The proposed modulator with OSR of 64 can achieve SNR of 151 dB. Finally, the modulator can achieve signal to noise ratio of 182 dB for OSR of 131 with full-scale input of the modulator is 550 mV. Due to CIFB topology, higher stability with multiple feedback structure. There is a demand for higher DC gain operational amplifier to achieve higher resolution. It is investigated that the operational amplifier has limited gain in DC, limited slew rate and gain bandwidth. Finally, the modulator is simulated for circuit non-idealities of thermal noise and flicker noise.

After the introduction, the second section discuss the design of the modulator design with CIFB topology, while the third section describes the modeling and simulation of the modulator and explain with reference to the non-idealities for the fourth-order multi-bit quantizer for discrete-time implementation. Finally, the section four concludes the paper.

2. MODULATOR DESIGN

A fourth-order multi-bit modulator modeled using Delta-Sigma Toolbox [12]. The CIFB investigated with higher out-of-band-gain (OBG). Also, to boost the performance of the modulator, the NTF

zero optimization techniques is employed. The CIFB topology can achieve SNR of 182 dB with oversampling ration (OSR) of 131. The CIFB topology allows higher stability with multiple to feedback. The NTF zero optimization causes more in-band quantization noise shaped to out-of-band. Without NTF zero optimization technique the modulator topologies can achieve SNR of 175 dB with OSR of 131 and OBG of 4. The CIFB modulator coefficient obtained from the toolbox shown in Table-I. This coefficient represents the ratio of

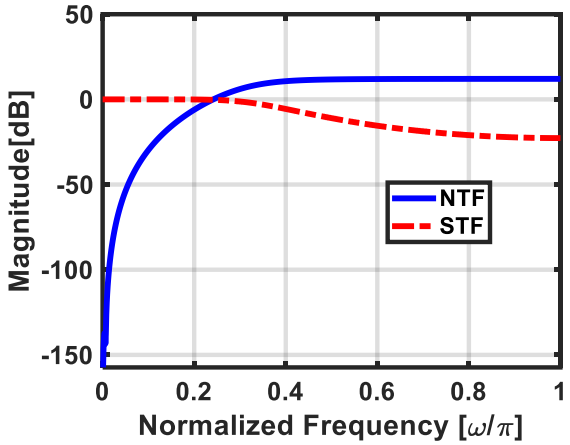

Figure 1: STF and NTF plot (CIFB)

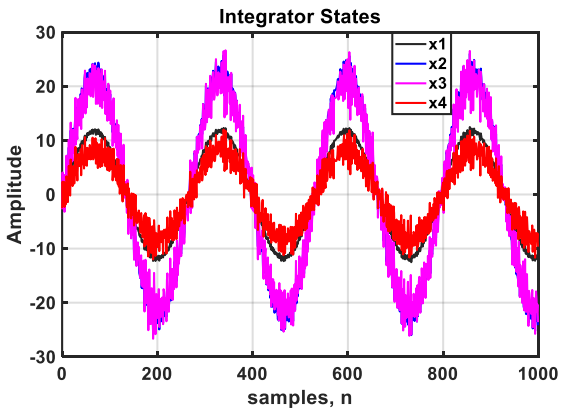

Figure 2: Integrator output states

capacitors at the switched-capacitor implementation, for the discrete-time implementation of the modulator. The noise transfer function (NTF) and signal-transfer function (STF) of the modulator are shown in Figure 1. The STF shows no peaking with smooth response as low pass filter response. While the NTF of the

Table I : CIFB Cofficients

Parameters	Values
a_1	0.292
a_2	1.421
a_3	2.744
a_4	2.553
b_1	0.292
g_1	0.0
g_2	0.000411

modulator shown in Figure 1 is a high pass response. While the Figure. 2 shows the output stages of each integrator, due to CIFB topology the swing inside the loop filter is large and it demands operational amplifier with high open loop DC gain. All operational amplifiers inside the loop filter are ideal have infinite gain to suppress the quantization noise in the signal band of the modulator. The fourth-order noise shaping modulator OBG gain also play an important role, which demands much higher value for 30-bit resolution. The Figure. 3 shows the STF is unity at the low frequencies while the NTF shows a high pass response at OBG value set to 4. The Figure. 4 shows the output power spectral density for CIFB topology of the modulator can achieve SNR of 181 dB with an OSR of 131. The Figure 4 shows the OBG value set to 4 for the case of NTF, while the STF have unity gain values according to the simulation environment.

3. NON-IDEALITIES SIMULATION

The ideal circuit modeling causes all integrator with very high DC gain while all the feedback path with fixed. To include the circuit non-idealities inside the loop filter as well as low resolution quantizer several non-ideal factors included, and

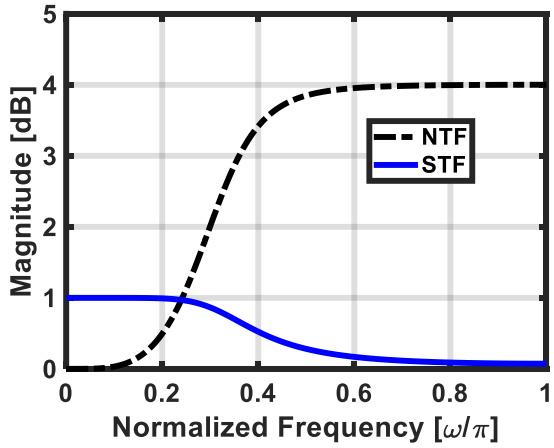

Figure 3: STF and NTF plot (CIFB)

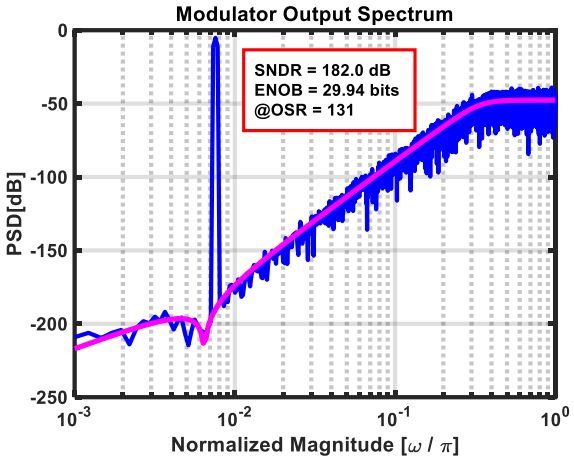

Figure 4: Output PSD plot (CIFB)

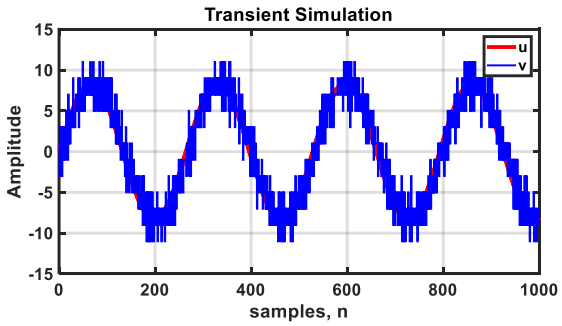

Figure 5: Multi-bit Output of the quantizer

complete circuit simulated to verify the functionality of the circuit using environment SD Toolbox [14]. Which simulates the circuit non-idealities are used? This section will discuss about the circuit non-idealities like thermal noise or kT/C, flicker noise, finite operational amplifier gain, finite slew-rate. The modulator can achieve fourth-order modulator with 4-bit quantizer can achieve signal-to-noise ratio (SNR) of 123 dB with OSR of 32. The proposed modulator with OSR of 64 can achieve SNR of 151 dB. Finally, the modulator can attain signal to noise ratio of 182 dB for oversampling ratio 131 with full-scale input of the modulator is 550 mV.

4. CONCLUSION

A high OSR fourth-order modulator designed for 30-bit resolution. The performance of the operational amplifier investigated for limited DC gain and other circuit non-idealities like thermal noise and flicker noise. The proposed modulator design investigated for different higher oversampling ratio like 128, 64, 32. The modulator can achieve fourth-order modulator with 4-bit quantizer can achieve signal-to-noise ratio (SNR) of 123 dB with OSR of 32. The proposed modulator with OSR of 64 can achieve SNR of 151 dB. Finally, the modulator can obtain SNR of 182 dB for OSR of 131 with full-scale input of the modulator is 550 mV. Due to CIFB topology, higher stability with multiple feedback structure. There is a demand for higher DC gain operational amplifier to achieve higher resolution. It is observed that the Operational amplifier has limited gain in DC, limited slew rate and the gain bandwidth. Finally, the modulator is simulated for circuit non-idealities of thermal noise and flicker noise.

5. ACKNOWLEDGMENT

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